REMARKS

This is in response to the Office Action dated December 26, 2007. Claims 13-14, 16-22, 24, 27-32, 34 and 36 are pending in the application. Claims 13, 24 and 31 are currently amended to more clearly describe the Applicant's invention as being a position based system, wherein the bits received by a node are determined by the position of the node in a string. Applicant respectfully submits that amendment to the claims merely clarifies the existing claims to explicitly recite a "position based" system. Since these limitations were already implicitly included in the claims, Applicant submits that no new matter is added by the current amendments and that the amendments do not necessitate new grounds for rejection.

Rejection under 35 U.S.C. §103(a)

Claims 13,14, 16-22, 24, 27-32 and 34-36 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,890,715 to Gomez et al. (hereinafter "Gomez") in view of U.S. Patent No. 3,675,196 to Molloy et al.

Claim 13, which is representative of the other rejected claims, recites:

> 13. A gaming system comprising:
> a plurality of devices to be individually accessed, arranged in a string of N nodes having first and second spaced ends, with each node including up to M of the devices, wherein M and N are whole numbers greater than one;
> a host controller directly connected to only the first end of the string and having a data out terminal;
> a plurality of local controllers respectively associated with the nodes,
> each local controller having a data in terminal and a data out terminal and **including a M-bit shift register with the register positions respectively connected to device output terminals to which the devices of the associated node may respectively be connected**;

the data out terminal of the host controller being connected to the data in terminal of a first node and the data in terminal of each of the other nodes being connected to the data out terminal of the preceding node in the string **so that the string of nodes provides a (MxN)-bit shift register**;

the host controller producing at its data out terminal **a position based output signal comprising a serial digital data stream including MxN bits followed by a strobe indicator so that the MxN bits are sequentially loaded into and respectively fill the positions of the (MxN)-bit register, wherein the bits received by a node are determined by the position of the node in the string**;

each local controller being responsive to the strobe indicator for utilizing the contents of its M-bit shift register for accessing the associated devices.

Gomez discloses "A pinball machine which can be electrically linked to other pinball machines." (Abstract). "When the machines are linked, one of the two machines is determined to be the master and the other the slave... messages are sent from one machine to the other machine when a certain feature on the machine is activated or wherein music or speech is started on that machine, so that appropriate action can be taken on the other machine, such as activating that feature or synchronizing the sound effects... When the feature is activated on one machine, a message is sent to the other machine containing data representing the feature activated. The UART transmits the message via the serial cable to the UART interface on the other machine. The UART interface on the other machine sends an interrupt message to the processor on the other machine to alert it to the incoming message. The microprocessor on the other machine then reads in the message from the UART interface, and activates the feature identified therein." (Col. 5, lines 25 – 67).

The Office Action erroneously asserts that Gomez teaches "each local controller... including a M-bit shift register with register positions respectively connected

to device output terminals..." Office Action page 3, lines 8 – 10. The Office Action also erroneously asserts that Gomez teaches the use of UART interfaces which comprise shift registers (figure 5b, col. 5, lines 50-67) wherein "the string of nodes provides a (MxN)-bit shift register (the daisy chain connections of the machines in figure 5b and the detailed description there of [sic] along with the discussions of the UART interfaces cited above.)" Office Action, page 3, lines 15 – 15.

Applicant respectfully submits that, contrary to the Examiner's assertion, the configurations described in Gomez merely recite conventional serial communication with well known UART interfaces. See col. 4, lines 24 – 34. While UART interfaces are well known to include shift registers, and are well known to be connected serially, such serially connected or daisy chained UARTs do not form Applicant's claimed MxN bit shift register wherein each M-bit node includes register positions to control devices on the node.

Gomez does not teach or suggest anything about an "M-bit shift register with the register positions respectively connected to device output terminals to which the devices of the associated node may respectively be connected" as particularly claimed. Rather, Gomez teaches that messages sent over the UART interfaces are address based and read by microprocessors in a conventional manner. For example, Gomez recites "[w]hen one machine sends a message to another machine via the serial interface, the message is passed from the Transmit serial terminal being used in each machine to the Receive serial terminal on the next machine. If the microprocessor on the receiving machine des not recognize the identification code stored in the message of the intended recipient, it passes the message on to the next machine in the ring in the same

manner...." Col. 8, 7, line 63 – col. 8, line 2. (See also col. 7, lines 30 – 32 describing addressed based messaging.) While the UARTs used by Gomez may include serially connected registers, they are not arranged as an MxN bit shift register as claimed. The register positions of the UARTs as described by Gomez are used conventionally, i.e., to store data and address information for processing by a microprocessor. This is in stark contrast to the position based communication that is enabled by Applicant's claimed MxN bit shift registers.

The Examiner admitted that "Gomez fails to explicitly recite the specifics of a serial digital data stream including MxN bits followed by a strobe indicator so that the bits are sequentially loaded into and respectively fill positions of the bit register." The Examiner asserted however that "in a related patent, Molloy teaches the use of shift registers in a position based system wherein a master controller communicates with local controllers and transmits pulse trains containing sets of data bits to receivers at all the associated devices wherein each of the devices (lights) is controlled by a specific bit in a specific set of bits transmitted by the master controller (abstract, 8:39-9:4, 11:60-12:30)." Office Action, page 3, line 19 – page 4, line.

Molloy discloses "[an] automobile traffic signal control system [which] controls traffic signals (lights) at a plurality of traffic intersections by way of a master controller which communicates with a local controller at each intersection and transmits pulse trains containing sets of data bits in sequence to the receivers at all the intersections, whereupon the intersection to which a specific set of data bits is addressed stores the set and uses each specific bit in the set to control a specific light or signal at that intersection. In this manner, all lights and signals at all intersections are specifically

each controlled by a specific bit in a specific set of bits transmitted by the master controller to the local controllers at the intersections." Abstract.

Contrary to the Examiner's characterization, Molloy does not describe a position based system, i.e., a system with a string of nodes which provides a (MxN)-bit shift register as claimed. Rather, Molloy recites:

> [a] two wire transmission line from the master controller to the local controllers carries all normal control signals transmitted for controlling the intersection lights. Trains of signals are transmitted over this line which carry therein the intersection address, as set of data bits for controlling the signal lights at the intersection and check signals...
>
> Col. 2, lines 53 – 59.
>
> The two element transmission line carries the data signals from the master controller to the first local controller which receives the signal train and simultaneously transmits it to a second local controller and meanwhile stores the set of data bits and address in the received signal train in a shift register. **The second local controller receives the same set** and address transmitted from the first local controller and also stores it in a shift register and transmits it to a third local controller and so forth. Thus, the set of data bits and address transmitted by the master controller is stored in each of the local controller. Then in the local controllers each local controller compares the received address with the local address while making a cyclic check for errors in the received set of data bits. If the received set of bits checks alright, the local controller **to which it is addressed** feed the data bits from the bits shift register to a buffer register that controls the lights... At the next transmission interval, the set of data bits is addressed to another local controller and is received by all of the local controllers replacing the previously received set and address stored in the shift registers in all of the local controllers...
>
> Col. 3, lines 1 – 21. Emphasis added by applicant.

Thus, Molloy discloses an address based system and does not disclose a position based system. And, since the second local controller of Molloy receives the same set of data as the first, Molloy is clearly distinct from the present invention wherein the set of data received by a node is determined by the position of the node in a series.

Thus, Applicant respectfully submits that neither Molloy nor Gomez alone or combined teach or suggest "serial digital data stream including MxN bits followed by a strobe indicator so that the MxN bits are sequentially loaded into and respectively fill the positions of the (MxN)-bit register" as particularly claimed by Applicant.

Applicant submits that the deficiencies of Molloy and Gomez described above apply to each of the rejected claims. Since neither Molloy nor Gomez, alone or combined teaches or suggests each and every element of claim 13 or any of the pending independent claims, Applicant respectfully submits that the rejections under 35 U.S.C. §103 are improper and should be withdrawn. Reconsideration is respectfully requested.

In view of the foregoing, it is submitted that as amended herein the application is now in condition for allowance. An early notice of allowance is respectfully requested.

Respectfully submitted,

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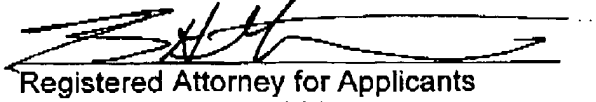

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